Soft Switched Multilevel Unidirectional High Frequency Link DC/AC converter for Medium Voltage Grid Integration

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***Abstract*—This paper describes a cascaded multilevel converter topology for direct medium voltage grid integration of photovoltaic sources. The topology uses high frequency magnetic isolation and hence, reducing volume and cost of overall system. The topology is single stage and does not have any inter-stage bulky filter capacitor, thus improving reliability. The low voltage DC side converter active switches are high frequency switched. These active switches are zero voltage switched (ZVS) for most part of the line cycle. The soft-switching is achieved without additional snubber elements. The active switches interfacing the medium voltage grid are switched at line frequency incurring negligible switching loss. The converter has modular structure which also has added advantages of easy repair-replacement. Modulation strategy and soft-switching technique are analyzed in detail. Key simulation results are presented to verify the circuit operation.**

NOMENCLATURE

V_{dc}	:Source DC Voltage.
V_o	:RMS output voltage (Line to Neutral).
V_g	:RMS grid voltage (Line to Neutral).
P	:Power output of a 1ϕ module.
I_o	:RMS output current.
v_o	:Instantaneous output voltage (Line to Neutral).
i_o	:Instantaneous output current (Line to Neutral).
N	:Total number of modules.
T_r	:Transformer turns ratio.
M	:Modulation Index.
f_{sw}	:Switching frequency.
f	:Grid frequency.

I. INTRODUCTION

With decreasing fossil fuel reserve and global warming scenario, nowadays power generation by renewable sources are gaining huge popularity [1]. Compared to hydro and wind, solar energy is becoming more popular as a source of renewable energy. Solar power is harvested in the form of DC. Furthermore, utilities are using medium or high voltage AC transmission grid for bulk power transmission as loss reduces greatly with increased voltage level. Conventionally, the photovoltaic (PV) DC output is first converted to 400V, 50/60 Hz AC and then the voltage level is stepped up using line frequency transformer (LFT) to connect to medium or high voltage Grid. The magnetic isolation also reduces ground leakage current of PV panel [2]. These LFTs are bulky, heavy and costly. Further, in conventional PV-grid integration, line filters are placed in low voltage side of the transformer leading to higher copper losses.

A popular alternative of line frequency magnetic isolation is using high frequency link (HFL) based converter topologies with reduced volume and cost of the overall system. Most commonly used HFL topologies are rectifier type (RHFL) [3], [4] and cyclo-converter type (CHFL) [5], [6]. In these topologies, switches are used in secondary side of the high frequency transformer (HFT) to convert HF AC to LF AC and hence, step-up capability of the HFT gets restricted since blocking voltage of commercially available semiconductor switches is limited to $4.5kV - 6.5kV$. A direct integration of medium voltage grid ($11kV/33kV$) with conventional HFL topologies is not possible due to this limitation. Direct grid integration of the converter reduces number of transformer stages needed for step up to medium voltage for grid integration which in turn reduces overall losses, size and cost of the system.

The multilevel topologies discussed in [7], [8] do not use high frequency isolation. In [9], [10] cascaded multilevel HFL multistage topologies are shown. In these topologies, isolated DC-DC stage is connected to VSI through inter stage filter capacitor and in AC side a number modules are connected in cascade to get the medium voltage output. The bulky inter stage filter capacitors cause reliability issue and all active switches are high frequency switched causing significant switching loss. In [11], a multilevel high frequency link (HFL) three phase single stage topology is shown for medium voltage grid integration of photovoltaic sources. The topology uses AC (four quadrant) switches in the grid side of the high frequency isolation. High voltage blocking AC switches are not commercially available and AC switches increase control complexity of the converter. Modulation strategy shows high frequency switching of all active switches. These will result in high switching loss of the converter. In [12] a novel multilevel HFL 3ϕ cascaded topology is shown. Here asymmetry in transformer turns ratio results in more voltage levels. Here also in the grid side AC switches are used and all the switches are HF switched.

In this paper, the proposed topology (as shown in Fig. 1) is a cascaded multilevel single stage 1ϕ converter with high

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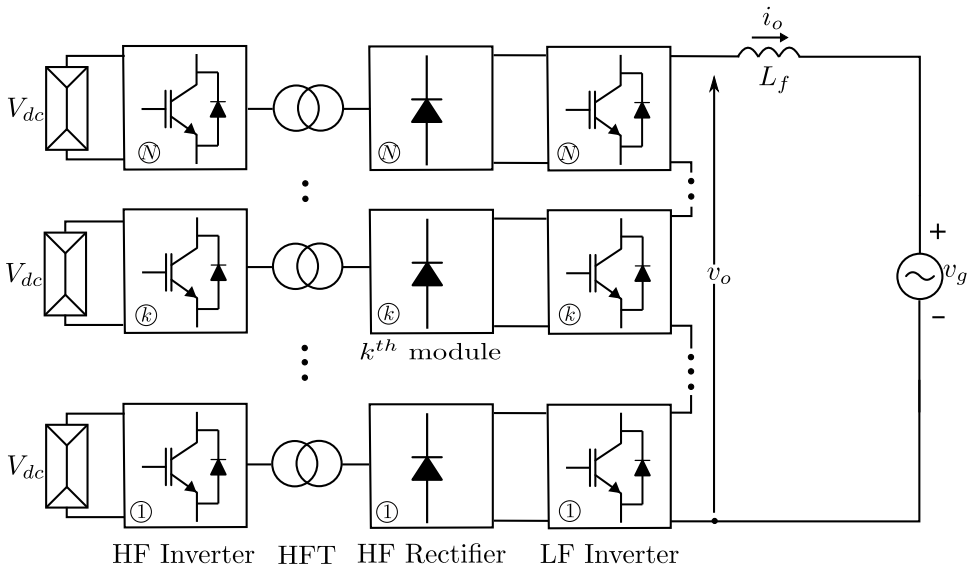

Fig. 1: Proposed Multilevel Topology (one phase of a 3ϕ system)

frequency isolation for direct medium voltage grid integration. The DC source can be a parallel connected DC supply or several isolated photovoltaic sources as shown in Fig. 1. Three such converters can be used for a 3ϕ connection where the modulation signals given by the controller will be 120° phase shifted. But the discussion on 3ϕ is beyond the scope of this paper. Commercially available high voltage blocking switches are used in each grid side converter module and by cascading the modules required medium voltage can be obtained. The switching speed of these AC side HV blocking active switches are relatively low incurring high switching loss if switched at high frequency. Modulation strategy of the converter ensures line frequency switching of these high voltage blocking switches. This modular structure also comes with easy repair and replacement of faulty module without much change in converter configuration. In the proposed topology, high frequency transformer is used for magnetic isolation and to get required voltage magnification. This reduces overall system volume and cost as compared to low frequency transformer. Due to presence of diode bridge in the circuit, power flow is unidirectional. DC side converter active switches are high frequency switched. The modulation strategy ensures zero voltage switching (ZVS) of high frequency switched DC side H-bridges.

The organization of the paper is as follows: Section-II presents modulation strategy and soft-switching process of the proposed converter. Section-III gives simulation results to verify the operation of the converter.

II. Modulation Scheme

In this topology, components used in all the modules are identical but modulation scheme is different for different modules. In this section, switching strategy for k^{th} module of the converter is described in details. The k^{th} module is shown in Fig. 2. This section is divided into two subsections:

- Pulse width modulation scheme

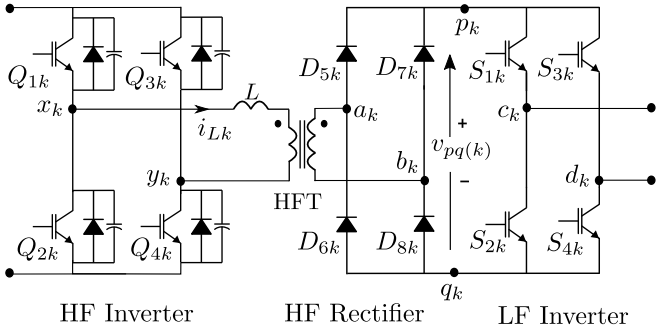

Fig. 2: k^{th} Module *(expanded)*

- Soft switching

A. Pulse Width Modulation Scheme

Pulse width modulated high frequency square wave is generated using HF inverter and applied across the transformer terminal of $x_k y_k$. The switch pair $Q_{1k} - Q_{2k}$ and $Q_{3k} - Q_{4k}$ (Fig. 2) are complementary switched with a deadtime as the switches are across the DC source. The subscript k indicates k^{th} module; $k \in [1, N]$. These pulses are high frequency (f_{sw}) square wave with 50% duty ratio. To generate PWM output, a phase shift is provided between the gating signal of Q_{1k} and Q_{3k}. The phase shift varies with time and is obtained from $m_k(t)$ where $m_k(t)$ is the modulation signal of k^{th} module. The gating signals are generated as follow: P is a square wave with frequency f_{sw} & 50% duty ratio. P is aligned with the carrier signal SC which is a periodic ramp with unity peak and $2f_{sw}$ frequency as shown in Fig. 3. Intermediate signal X is given as

$$X = \begin{cases} 1, & m_k(t) \leq SC \\ 0, & m_k(t) > SC \end{cases} \tag{1}$$

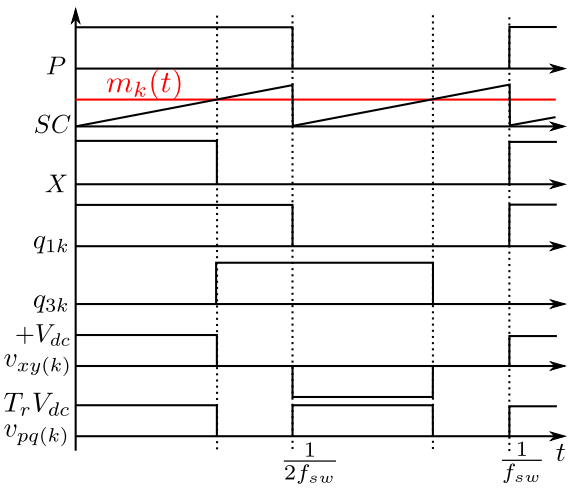

Fig. 3: Switching strategy of HF inverter

The gating signals q_{1k} and q_{3k} of switches Q_{1k} and Q_{3k} are given as

$$q_{1k} = P \tag{2}$$

$$q_{3k} = q_{1k} \oplus X \tag{3}$$

This switching strategy applies a pulse width modulated high frequency square wave across $x_k y_k$. From Fig. 2 and Fig. 3, the pulse width of $v_{xy(k)}$ is proportional to magnitude of $m_k(t)$ where $m_k(t) \in [0, 1]$.

The output of HF inverter is fed to a HF diode bridge rectifier through a HFT whose output averaged over a switching cycle $< v_{pq(k)}(t) >$ is given as

$$< v_{pq(k)}(t) >= m_k(t) T_r V_{dc}, \qquad m_k(t) \in [0, 1] \tag{4}$$

Throughout this paper, the symbol $<>$ represents a quantity averaged over a switching cycle ($\frac{1}{f_{sw}}$). Next, the generation of $m_k(t)$ is discussed in details.

Fig. 4 shows the equivalent circuit of the converter integrated with the AC grid through a line filter (L_f) and the corresponding phasor diagram. As the power flow of the converter is unidirectional (DC to AC) due to presence of diode bridge rectifier, $< v_o(t) >$ and $< i_o(t) >$ must be in phase. From the phasor diagram, V_o is given as:

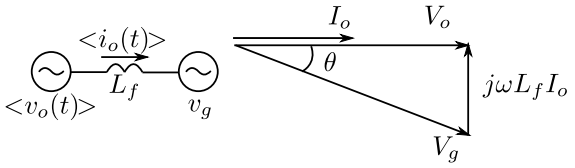

Fig. 4: Equivalent circuit of the converter connected with the grid

$$V_o = (j\omega L_f) I_o + V_g \tag{5}$$

Active power P is given as-

$$P = V_o I_o = V_g I_o \cos\theta = \frac{V_g V_o}{\omega L_f} \sin\theta \tag{6}$$

where $\omega = 2\pi f$ and θ is phase angle difference between $< v_o(t) >$ and $v_g(t)$. Solving 5 & 6, V_o, θ and $< v_o(t) >$ are given as-

$$V_o = \left(\frac{V_g^2}{2} + \sqrt{\frac{V_g^4}{4} - (\omega L_f P)^2} \right)^{1/2} \tag{7}$$

$$\theta = \sin^{-1}\left(\frac{\omega L_f P}{V_g V_o} \right) \tag{8}$$

$$< v_o(t) >= V_p \sin(\omega t + \theta) \tag{9}$$

where V_p is $\sqrt{2} V_o$. Based on $< v_o(t) >$, an intermediate signal $m(t)$ is defined such that $m(t)$ is in phase with $v_o(t)$ and has a peak equal to the total number of modules N.

$$m(t) = N |\sin(\omega t + \theta)| \tag{10}$$

In actual closed loop control implementation, the controller provides $m(t)$ by sensing $v_g(t)$ and $i_o(t)$ for a given power demand P.

At a given instant of time if $k-1 < m(t) < k$, modulation signals of different modules are given as-

$$m_j(t) = \begin{cases} M(m(t) - (k-1)), & j = k \\ M, & j \in [1, k-1] \\ 0, & j \in [k+1, N] \end{cases} \tag{11}$$

where $m_j(t)$ is the modulation signal of j^{th} module as shown in Fig. 5.

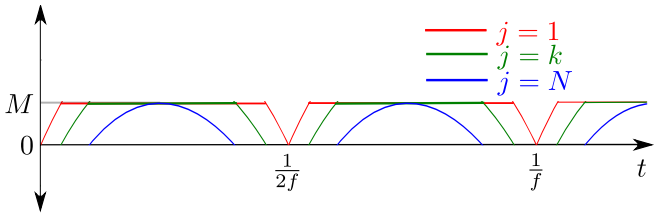

Fig. 5: $m_j(t)$ for $j = 1, k, N$

From (4) and (11), obtained switching cycle average of the diode rectifier outputs $< v_{pq(j)}(t) >$ are shown in Fig. 6.

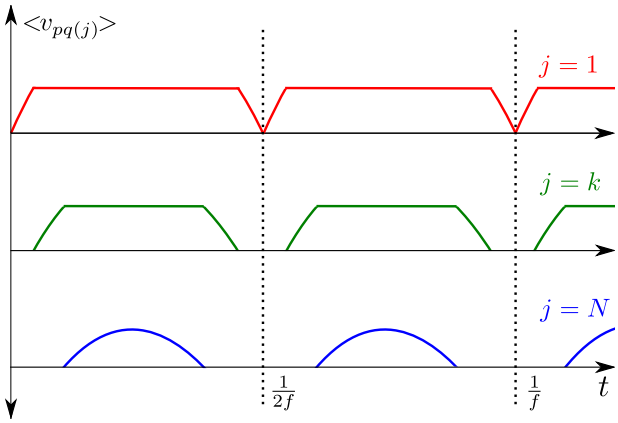

Fig. 6: $v_{pk(j)}(t)$ for $j = 1, k, N$

Using (4) & (11), cumulative average output voltage of diode bridge rectifiers of N modules is given as-

$$\begin{aligned}&\sum_{j=1}^{N} < v_{pq(j)}(t) > \\ &= \sum_{j=1}^{k-1} < v_{pq(j)}(t) > + < v_{pq(k)}(t) > + \sum_{j=k+1}^{N} < v_{pq(j)}(t) > \\ &= T_r V_{dc}(M(k-1) + M(m(t) - (k-1))) + 0 \\ &= m(t) M T_r V_{dc}\end{aligned} \tag{12}$$

Output of these rectifiers are fed to line frequency inverters to get bipolar output voltage. The gating signals of line frequency inverter in k^{th} module are given as-

$$s_{1k} = s_{4k} = \begin{cases} 1, & < v_o(t) > is + ve \\ 0, & otherwise \end{cases} \tag{13}$$

$$s_{2k} = s_{3k} = \overline{s_{1k}} \tag{14}$$

Due to cascade connection, output of the line frequency inverters are summed up resulting total output voltage $v_o(t)$. From (13) & (14), all the LF inverter are synchronously switched. Hence,

$$< v_o(t) > = \begin{cases} + \sum_{j=1}^{N} < v_{pq(j)}(t) >, & 0 < \omega t + \theta < \pi \\ - \sum_{j=1}^{N} < v_{pq(j)}(t) >, & \pi < \omega t + \theta < 2\pi \end{cases} \tag{15}$$

From (10), (12) & (15) average output voltage is given as-

$$< v_o(t) > = M N T_r V_{dc} \sin(\omega t + \theta) \tag{16}$$

The modulation index M is selected such that

$$M = \frac{\sqrt{2} V_o}{N T_r V_{dc}} \tag{17}$$

Due to the presence of leakage inductance, there is a finite current commutation time of diode bridge rectifier leading to loss in duty cycle resulting drop in output voltage which is adjusted in the modulation strategy.

During the interval when $m_k(t) = 0$, output voltage of the HF inverter is zero. During this interval, all switches of the HF inverter of k^{th} module are turned off in order to freewheel the load current through diode bridge rectifier resulting reduced losses in HF inverters and HFTs.

B. Soft Switching Scheme

The high frequency switched DC side converters are zero voltage switched for most part of the line cycle. This improves overall system efficiency. The soft switching is achieved mainly using device capacitance and transformer leakage inductance. What follows is a brief description of zero voltage switching process of k^{th} module HF inverter. The equivalent circuit is shown in Fig. 7. The high frequency inverter is switched to apply $\pm V_{dc}$ and zero voltage across the transformer terminal $x_k y_k$. To apply a zero voltage from $+V_{dc}$ or $-V_{dc}$, $Q_{3k} - Q_{4k}$ are switched. To apply $+V_{dc}$ or $-V_{dc}$ from zero $Q_{1k} - Q_{2k}$ are switched. These results four

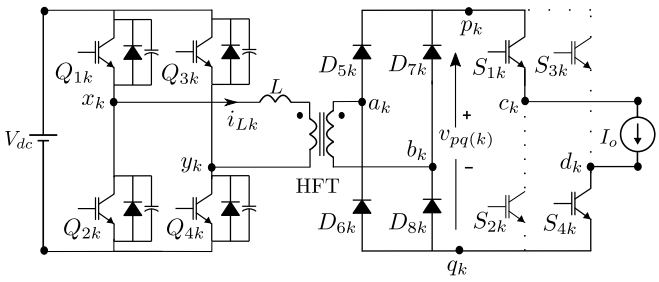

Fig. 7: Equivalent circuit diagram to describe soft switching process of the HF inverter (k^{th} module)

switching transitions over a switching cycle ($\frac{1}{f_{sw}}$) (Fig. 8). Here Q_{4k} to Q_{3k} transition (to apply $+V_{dc}$ to zero across $x_k y_k$) and Q_{1k} to Q_{2k} transition (to apply zero to $-V_{dc}$ across $x_k y_k$) are discussed in detail. Other two transitions are

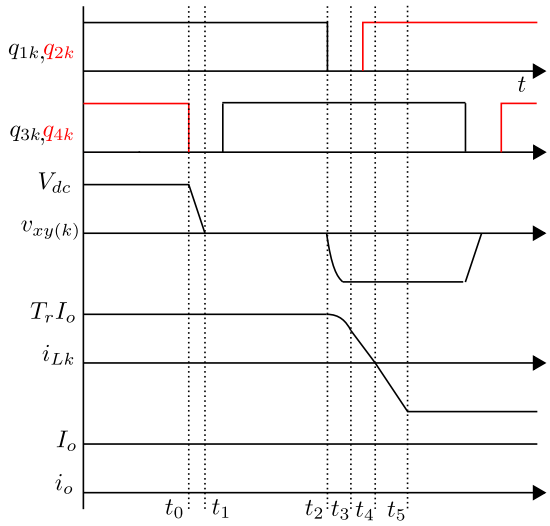

Fig. 8: Switching transitions in HF inverter of k^{th} module

very similar. Switching waveforms are shown in Fig. 8. To simplify the switching analysis slowly varying filtered output current is considered as constant current source I_o over a switching cycle (see Fig. 7). C_{1k}-C_{4k} are the capacitors across the devices Q_{1k}-Q_{4k} and the anti-parallel diodes are denoted as D_{1k}-D_{4k} respectively.

1) Q_{4k} to Q_{3k} switching transition (Fig. 8): Before this transition the switches Q_{1k}, Q_{4k} are conducting and $+V_{dc}$ is applied across the $x_k y_k$. Transformer current i_{Lk} is positive as shown in Fig. 7. In load side diode bridge D_{5k} and D_{6k} are conducting. At $t = t_0$, the switch Q_{4k} is turned off. Due to presence of device capacitance C_{4k}, voltage across Q_{4k} can not change immediately. The voltage starts to build up after the channel current falls to zero. This results zero voltage turn off (ZVS) of Q_{4k}. Transformer current i_{Lk} starts charging C_{4k} and discharging C_{3k} Initial conditions are- $v_{C3k}(t_0) = V_{dc}$, $v_{C4k}(t_0) = 0$ and $i_{Lk}(t_0) = T_r I_o$. The dynamics of capacitor voltages are given as-

$$v_{C3k} = V_{dc} - \frac{T_r I_o}{2C} t \tag{18}$$

$$v_{C4k} = \frac{T_r I_o}{2C} t \tag{19}$$

where $C_{3k} \simeq C_{4k} \simeq C$ and L is the leakage inductance of the transformer. At $t_1 = \frac{2CV_{dc}}{T_r I_o}$, C_{3k} is completely discharged. D_{3k}, anti-parallel diode of Q_{3k} is forward biased and starts conducting. As Q_{1k} and body diode of D_{3k} are conducting, a zero voltage is applied across $x_k y_k$. This is a freewheeling state or zero state i.e. no active power is transferred in this state. In order to get zero voltage turn on, gating pulse of Q_{3k} is applied when D_{3k} is conducting.

2) Q_{1k} to Q_{2k} switching transition (Fig. 8): At the end of zero state at $t = t_2$, Q_{1k} is turned off. Due presence of C_{1k}, this turn off is also a zero voltage transition like Q_{4k} explained in last section. i_{Lk} starts charging C_{1k} and discharging C_{2k}. The circuit condition applies a negative voltage across $x_k y_k$. The applied voltage polarity of the transformer forward biases D_{6k} and D_{7k} of the diode bridge. All four diodes are in conduction applying a short across the transformer terminals $a_k b_k$. The equivalent circuit during this interval is shown in Fig.9. Initial conditions are- $v_{C1k}(t_2) = 0$, $v_{C2k}(t_2) = V_{dc}$, $v_{x_k y_k}(t_2) = 0$, $i_{Lk}(t_2) = T_r I_o$. By analyzing circuit in Fig.9, the dynamic

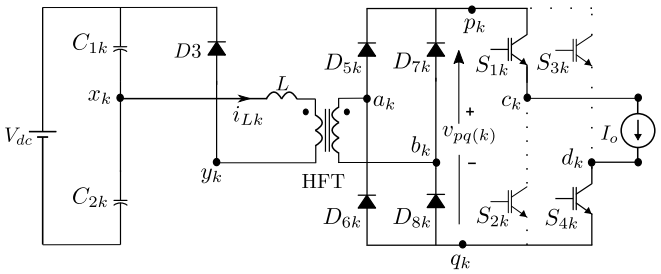

Fig. 9: Equivalent circuit diagram during Q_{1k} to Q_{2k} switching transition

equations of transformer current and capacitor voltages are given as:

$$i_{Lk} = T_r I_o \cos\left(\frac{t}{\sqrt{2LC}}\right) \tag{20}$$

$$v_{C1k} = T_r I_o \sqrt{\frac{L}{2C}} . \sin\left(\frac{t}{\sqrt{2LC}}\right) \tag{21}$$

where $C_{1k} \simeq C_{2k} \simeq C$. In order to completely discharge the capacitor C_{2k}, $T_r I_o \sqrt{\frac{L}{2C}} \geq V_{dc}$. This condition limits the range soft-switching over full line cycle. At t_3, C_{2k} is completely discharged. Anti-parallel diode D_{2k} starts to conduct and $-V_{dc}$ is applied across L. i_{Lk} starts falling linearly with a slope of V_{dc}/L. To achieve zero voltage turn on, gating signal of Q_{2k} is applied during this sub-interval. At t_4, i_{Lk} becomes zero. After t_4, i_{Lk} becomes negative continues to fall with same slope. Now switch Q_{2k} and Q_{3k} are conducting. At t_5, i_{Lk} is equal to $-T_r I_o$. At this instant D_{5k} and D_{8k} stop conducting and are reverse biased. A negative voltage $-V_{dc}$ is applied across $a_k b_k$ which completes the zero to active state transition.

III. Simulation Results

The proposed topology is simulated in MATLAB simulink. Simulation parameters are given as follows.

Parameter	Value
DC Bus Volatge (V_{dc})	$800V$
RMS Grid Voltage (V_g)	$(11/\sqrt{3})kV$
Rated 1ϕ Power (P)	$3.33kW$
Number of modules (N)	5
Transformer turns ratio (T_r)	2.5
Switching frequency (f_{sw})	$20kHz$
Grid frequency (f)	$50Hz$
Leakage inductance (L)	$320\mu H$
Capacitance across devices (C)	$160pF$
Deadtime $(t_{deadtime})$	$1\mu s$
Phase angle (θ)	$3.32°$

Fig. 10 shows converter output voltage $v_o(t)$, current $i_o(t)$ and grid voltage $v_g(t)$. Five levels seen in $v_o(t)$ are due to cascading of five modules to get the required output voltage. The fundamental component of v_o and i_o are in phase ensuring UPF operation of the converter. There is a phase lag of θ between i_o and v_g. From simulation, the peak value of v_g is $8.94kV$. Theoretical peak value of v_g is $8.98kV$. This drop is due to non-idealities of the components used in simulation. Fig. 11 shows diode bridge

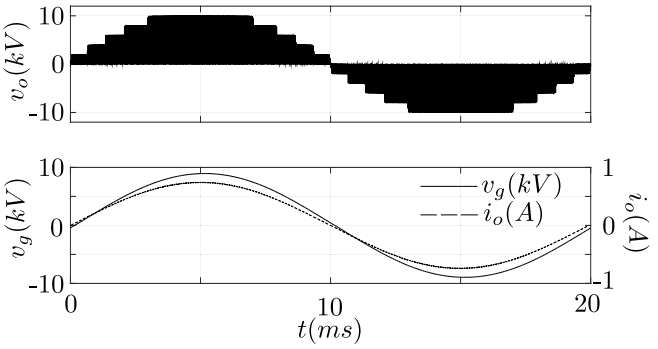

Fig. 10: Simulated waveforms of $v_o(t)$ and $i_o(t)$

output $v_{pq(j)}$ for $j = 1, 3 \& 5$ and cumulative output of these voltages, showing the cascade nature of the converter to generate five level output voltage. Fig. 12 shows high frequency transformer input currents $i_{Lj}(t)$ for $j = 1,3$ and 5. $i_{Lj} \approx 0$ in the zone where $m_j(t) = 0$ for a module. This figure confirms that the load current circulate through the secondary diode bridge when $m_j(t) = 0$. Load current doesn't contribute to any loss in transformer and HF inverter during $m_j(t) = 0$. Fig. 13 shows input voltage to the diode bridge and transformer magnetizing current of module 1. Magnetization current of transformer (i_{mag}) doesn't have any DC component, implying flux-balance over a switching cycle. Fig. 14 shows soft switching waveform of module 1. During active to zero state transition $Q_{31} - Q_{41}$ are switched. $v_{xy(1)}$ falls to zero when Q_{41} is turned off. After some time of this transition, Q_{31} is turned on when the body diode of

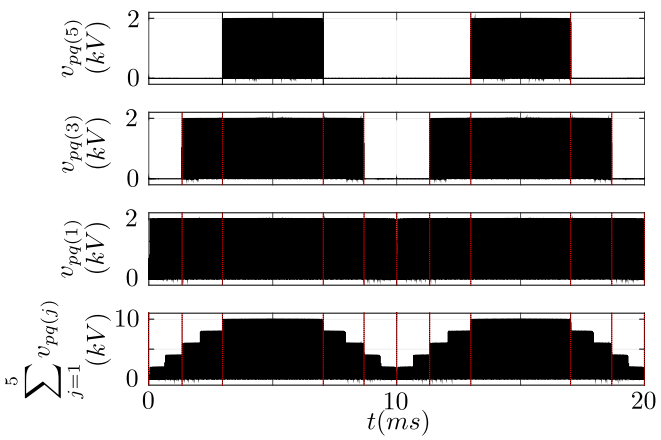

Fig. 11: Simulated waveforms of $v_{pq(j)}$ for $j = 1$, 3 & 5 and cumulative output of all $v_{pq(j)}$

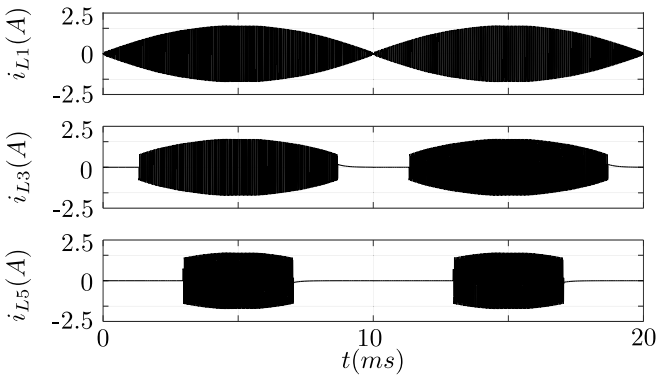

Fig. 12: Simulated waveforms of $i_{Lj}(t)$ for $j = 1$, 3 and 5

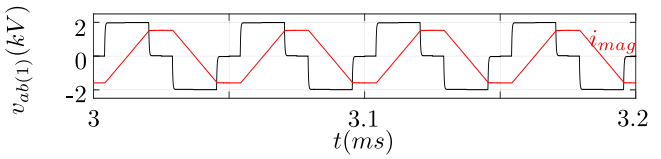

Fig. 13: Simulated waveforms showing HFT input voltage, current, magnetizing current of module 1

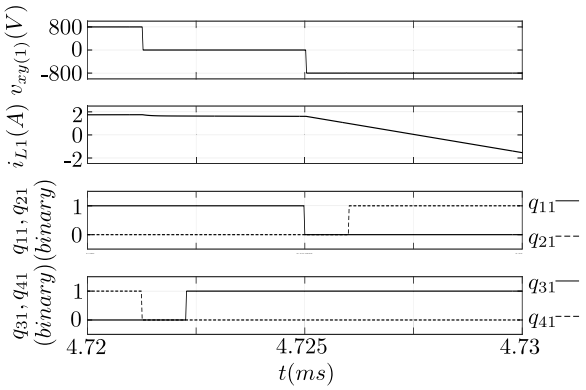

Fig. 14: Simulated waveforms showing soft switching

Q_{31} was conducting. This ensures ZVS turn on of Q_{31}. In case of zero to active state transition $Q_{11}-Q_{21}$ are switched. After turn off of Q_{11}, $v_{xy(1)}$ becomes -800V. After that when the body diode of Q_{21} is conducting, gating signal is applied to Q_{21} ensuring ZVS turn on.

IV. Conclusion

In this paper, a cascaded multilevel converter topology for direct DC/AC medium voltage grid integration along with its modulation scheme is proposed. The key features of the proposed topology are: (a) with exiting semiconductor technology, proposed topology gives a solution for direct integration of medium voltage grid. (b) the use of HF transformer isolation reduces overall system volume. (c) soft switching of HF inverter improves the system efficiency. (d) line frequency switching of high voltage blocking switches reduces system loss. It is seen from Fig. 12, all modules are not equally stressed. In future, an algorithm will be developed ensuring equal stress in all the module. This modular structure has added advantage of easy repair and replacement.

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